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1 V Electronically Tunable Differential Difference Current Conveyors Using Multiple-Input Operational Transconductance Amplifiers

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Abstract: This paper presents electronically tunable current conveyors using low-voltage, low-power, multiple-input operational transconductance amplifiers (MI-OTAs). The MI-OTA is realized using the multiple-input bulk-driven Metal Oxide Semiconductor transistor (MIBD-MOST) technique to achieve minimum power consumption. The MI-OTA also features high linearity, a wide input range, and a simple Complementary Metal Oxide Semiconductor (CMOS). Thus, high-performance electronically tunable current conveyors are obtained. With the MI-OTA-based current conveyor, both an electronically tunable differential difference current conveyor (EDDCC) and a second-generation electronically tunable current conveyor (ECCII) are available. Unlike the conventional differential difference current conveyor (DDCC) and second-generation current conveyor (CCII), the current gains of the EDDCC and ECCII can be controlled by adjusting the transconductance ratio of the current conveyors. The proposed EDDCC has been used to realize a voltage-to-current converter and current-mode universal filter to show the advantages of the current gain of the EDDCC. The proposed current conveyors and their applications are designed and simulated in the Cadence environment using 0.18 µm TSMC (Taiwan Semiconductor Manufacturing Company) CMOS technology. The proposed circuit uses ±0.5 V of power supply and consumes 90 µW of power. The simulation results are presented and confirm the functionality of the proposed circuit and the filter application. Furthermore, the experimental measurement of the EDDCC implemented in the form of a breadboard connection using a commercially available LM13700 device is presented.

Keywords: second-generation current conveyor (CCII); differential difference current conveyor (DDCC); operational transconductance amplifier (OTA); voltage-to-current converter; current-mode universal filter

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1. Introduction

In the last decade, more and more attention has been paid to the current-mode technique in electronic circuit design. This technique can offer advantages in certain applications in terms of high-speed operation, bandwidth, accuracy, and simplified signal processing. Arithmetic operations, such as the addition, subtraction, and multiplication of signals in current forms are simpler compared to voltage-mode circuits. In other words, the addition and subtraction of signals in voltage forms based on operational amplifiers (op-amps) suffer from many passive resistors [1]. Moreover, current-mode circuits can be designed almost exclusively using current-mode devices because they do not need high current gain or high-precision passive elements. For example, an op-amp-based inverting amplifier offers a high-precision transfer function when there is high voltage gain (infinite for the ideal case) and high-precision passive elements are available [1].

Second-generation current conveyors (CCII) [2] are well-known active devices for realizing current-mode circuits, such as current-mode filters [3–6], current-mode oscillators [7–10], and current-mode rectifiers [11–13]. Furthermore, there are several current conveyors available according to the open literature, such as differential difference current conveyors (DDCC) [14], differential voltage current conveyors (DVCC) [15], fully differential current conveyors (FDCCII) [16], and fully balanced second-generation current conveyors (FBCCII) [17]. These current conveyors [14–17] are designed to enhance performance in terms of holding the input signals and/or output signals in differential forms.

Nowadays, CMOS active devices operating with low supply voltage and power consumption are of interest because they are required for applications in portable electronics, sensors, and biomedical systems. Power consumption is also a key parameter for researchers in the design of conventional electronic circuits. Focusing on current conveyors, low-voltage and low-power current conveyors are available according to the open literature, i.e., CCII in [18–20], DDCC in [21,22], FDCCII in [23–25], and FBCCII in [26–28].

A conventional CCII usually has three terminals (x-, y-, and z-terminals) [2], and its terminal relationships are $v_y = v_x$ and $i_z = i_x$. It should be noted that the voltage and current gains of a conventional CCII are equal to one. To increase the functionality of the CCII by offering electronic tuning of the current gain between the x- and z-terminals, electronically tunable CCIIs (ECCIIs) have been proposed [29–36]. In [29], the ECCII was first designed using an op-amp and an operational transconductance amplifier (OTA). ECCIIs can also be implemented using bipolar technology [30,31] and CMOS technology [32–34]. An electronically tunable differential difference current conveyor (EDDCC) was also proposed in [35,36]. The ECCIIs and EDDCCs are used as the basic building blocks of universal filters [37–40] and oscillators [41–47]. The current gain of the current conveyors can be used as a design parameter for applications, such as tuning the quality factor of the filters [37–39], adjusting the current gain of filter functions [40], selecting a single circuit to operate as either a filter or an oscillator [41], and controlling the condition of oscillation and/or the oscillator's frequency of oscillation [42–47]. It should be noted that the ECCII and EDDCC in [29–36] do not provide low-voltage and low-power operations, i.e., ±1.5 V of supply voltage [33], ±2.5 V of supply voltage [34,35], and ±5 V of supply voltage [31,36]. Although the current conveyors in [18–28] provide low-voltage and low-power operations, the current gain between the x- and z-terminals of these current conveyors is not provided.

Therefore, this paper presents low-voltage low-power current conveyors that offer current gain between the x- and z-terminals. The electronically tunable current conveyors have been designed using low-voltage, low-power, multiple-input OTAs (MI-OTAs). The current gain of the proposed electronically tunable current conveyor can be controlled by adjusting the ratio of transconductances of the current conveyors. The MI-OTA is realized using the multiple-input bulk-driven MOS transistor (MIBD-MOST) technique to obtain minimum voltage supply and power consumption [48]. Recently, multiple-input OTAs have been utilized in many interesting applications that exhibit a minimal number of active elements, power supply, and reduced complexity [48,49]. By using a MI-OTA-based electronically tunable current conveyor, we can obtain an electronically tunable differential difference current conveyor (EDDCC) and an electronically tunable second-generation current conveyor (ECCII). The EDDCC has been used to realize the voltage-to-current (V-to-I) converter and current-mode universal filter. The performances of the proposed current conveyors and their applications were evaluated in the Cadence environment using 0.18 μm CMOS technology from TSMC. The proposed current conveyors use ±0.5 V of power supply and consume 90 μW of power. The EDDCC has also been implemented in the form of a breadboard connection in order to perform experimental measurements. The proposed EDDCC can be used for voltage- and current-mode sensor applications or as a conditioning circuit for processing biological signals that require low supply voltages and reduced power consumption.

The paper is organized as follows: Section 2 describes the structure of the MI-OTA and the proposed EDDCC. The applications of the EDDCC as a V-to-I converter and current-mode universal filter are shown in Section 3. The simulation results of the proposed ECCII, the V-to-I converter, and the universal filter are shown in Section 4. Section 5 describes the experimental measurement results of the EDDCC. Finally, Section 6 concludes the paper.

2. Proposed Electronically Tunable Current Conveyors

2.1. The Multiple-Input Operational Transconductance Amplifier

The symbol and the CMOS realization of the multiple-input OTA proposed in this work are shown in Figure 1a and 1b, respectively. The output current I_{out} can be described by the following equation:

$$I_{out} = g_m(V_{+1} + V_{+2} - V_{-1} + V_{-2}) \tag{1}$$

where g_m is the small-signal transconductance.

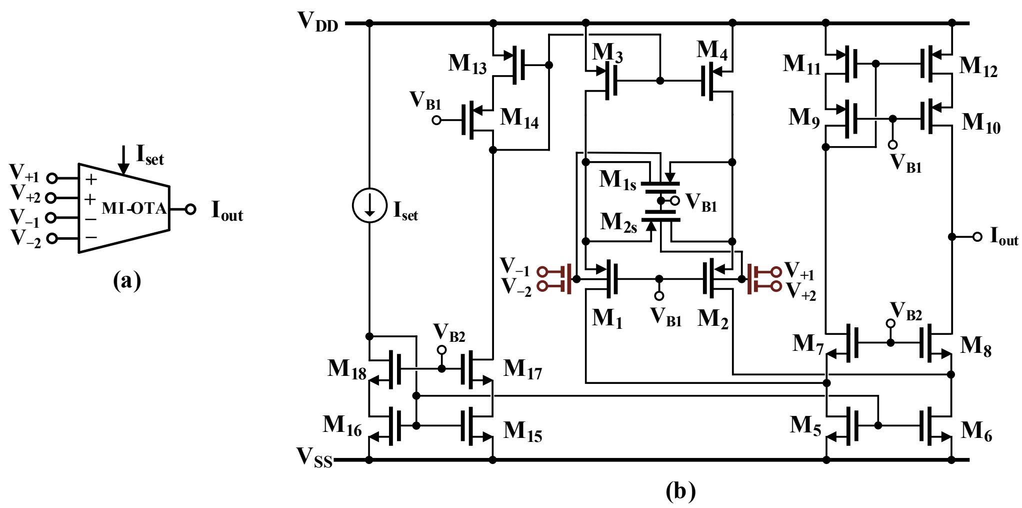


Figure 1. MI-OTA (**a**) symbol and (**b**) realization using the MIBD-MOST technique.

Overall, the circuit can be considered as a folded cascode OTA, with the input bulk-driven differential pair M_1, M_2 linearized using the triode region transistors M_{1s} and M_{2s}. A similar linearization technique was proposed by Krummenacher and Joehl [50] for a gate-driven transconductor operating in the strong inversion region. Figure 1 presents a BD counterpart of the circuit, operating in weak inversion, and with the input transistors replaced by multiple-input devices. Such a version of the input stage was first proposed and verified experimentally in [49].

The practical realization of multiple-input devices is shown in Figure 2. Note that multiple inputs were realized using a capacitive voltage divider/analog summer, composed of the capacitors C_{Bi}. The large resistors R_{MOSi}, connected in parallel to the capacitors, are used to properly bias the bulk terminal of the transistor for DC. They are realized as an anti-parallel connection of two minimum-size MOS transistors operating in the cut-off region. Due to their high resistances, their impact on the voltage transfer function of the input divider can be neglected for working frequencies of $\omega > 1/C_{Bi}R_{MOSi}$. In such a case, the AC voltage at the bulk terminal of the device can be expressed as follows:

$$V_b = \sum_{i=1}^{n} \beta_i V_i \tag{2}$$

where n is the number of inputs and β_i is the voltage gain of the input capacitive divider from *i*th input. Neglecting second-order effects, β_i can be expressed as follows:

$$\beta_i = \frac{C_{Bi}}{\sum_{i=1}^{n} C_{Bi}} \tag{3}$$

Note that with identical C_{Bi}, $\beta_i = 1/n$ for $i = 1, \ldots, n$.

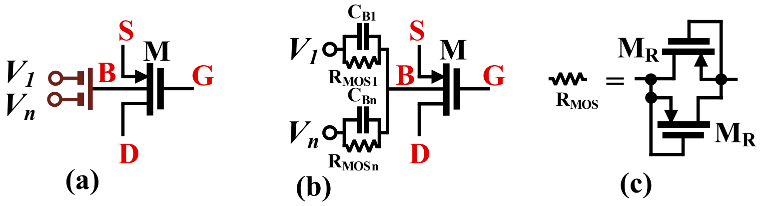


Figure 2. MIBD-MOST technique (**a**) symbol, (**b**) realization, and (**c**) R_{MOS} realization.

The MOS transistor with a capacitive input divider can be seen as a new active device called a bulk-driven multiple-input MOS transistor [48]. The use of such devices enables the realization of input signal summation (see Equation (1)) without the need for a second input stage, thus simplifying the overall structure and saving dissipated power.

Regarding the input stage of the OTA, its linearity depends on the parameter *k*, which is defined as follows:

$$k = \frac{(W/L)_{1s,2s}}{(W/L)_{1,2}} \tag{4}$$

The best linearity of the input stage is achieved for $k = 0.5$ [49], i.e., the same value as for its GD counterpart operating in weak inversion [51]. This result does not depend on the value of the biasing current I_{set} if the operation in weak inversion is provided.

The rest of the OTA structure is rather conventional, with its cascode output stage M_5-M_{12}. The transistors M_{13}-M_{18} are used for biasing purposes. All the transistors in the OTA circuit, except M_{1s} and M_{2s}, should operate in the penthode region.

The small-signal transconductance of the OTA can be expressed as follows [49]:

$$g_m = \beta \cdot \eta \frac{4k}{4k+1} \cdot \frac{I_{set}}{n_p U_T} \tag{5}$$

where $\eta = g_{mb1,2}/g_{m1,2}$ is the bulk-to-gate transconductance ratio of the input pair at the operating point, n_p is the subthreshold slope factor for p-channel devices, U_T is the thermal potential, and the other symbols are explained earlier.

As can be concluded from (5), the resulting transconductance is attenuated by the input capacitive divider and by the application of bulk-driven devices (note that both the capacitive divider gain β and the bulk-to-gate transconductance ratio η are less than unity). The transconductance is proportional to the biasing current I_{set}, and thus can be linearly regulated by this current.

The relatively low value of the overall transconductance also decreases the voltage gain of the OTA. However, thanks to the high-resistance cascode output stage, the DC voltage gain of the OTA is maintained at a sufficient level as follows:

$$A_V \cong g_m[(g_{m8} r_{ds8} r_{ds6})||(g_{m10} r_{ds10} r_{ds12})] \tag{6}$$

The input capacitive divider, as well as the bulk-driven technique, extend the linear range of the OTA $1/(\beta\eta)$ times. However, the input-referred noise is increased in the same proportion; thus, the dynamic range of the circuit remains unchanged as compared to its GD counterpart. Nevertheless, application of the bulk-driven technique, combined with an additional capacitive divider, simplifies the design of analog blocks in an ultra-low-voltage environment and avoids hard nonlinearities for a relatively large input voltage swing.

2.2. Proposed Electronically Tunable Current Conveyors

Figure 3a shows the symbol of the electronically tunable second-generation current conveyor (ECCII) and Figure 3b shows the electrical symbol of the electronically tunable differential difference current conveyor (EDDCC). The port characteristics of the ECCII and EDDCC can be expressed, respectively, as follows:

$$\begin{pmatrix} I_y \\ V_x \\ I_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm k & 0 \end{pmatrix} \begin{pmatrix} V_y \\ I_x \\ V_z \end{pmatrix} \tag{7}$$

$$\begin{pmatrix} I_{y1} \\ I_{y2} \\ I_{y3} \\ V_x \\ I_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & \pm k & 0 \end{pmatrix} \begin{pmatrix} V_{y1} \\ V_{y2} \\ V_{y3} \\ I_x \\ V_z \end{pmatrix} \tag{8}$$

The characteristics of the ECCII and EDDCC are similar to the conventional CCII [2] and DDCC [14], except for the current gain between the x- and z-terminals, which can be given by k.

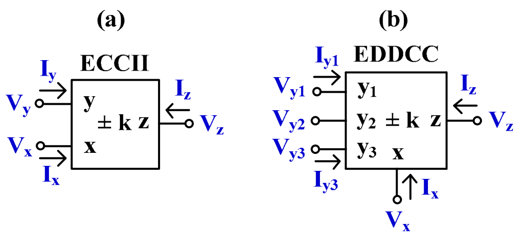


Figure 3. The symbol of electronically tunable current conveyors (**a**) ECCII and (**b**) EDDCC.

Figure 4 shows the proposed EDDCC using MI-OTAs. This circuit can also work as an ECCII if the y_1-terminal is the input and the y_2- and y_3-terminals are connected to ground. It can further work as an inverting ECCII if the y_2-terminal is the input and the y_1- and y_3-terminals are connected to ground.

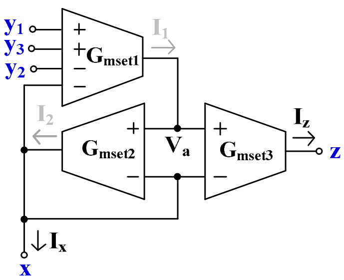


Figure 4. Proposed EDDCC using MI-OTAs.

To explain the operation of the proposed EDDCC, it is assumed that all OTAs are identical. Using (1), the currents I_1, I_2, and I_3 in Figure 4 can be expressed as follows:

$$I_1 = G_{mset1}\left(V_{y1} - V_{y2} + V_{y3} - V_x\right) \tag{9}$$

$$I_x = G_{mset2}(V_a - V_x) \tag{10}$$

$$I_z = G_{mset3}(V_a - V_x) \tag{11}$$

The OTA_2 of G_{mset2} is connected as a negative-feedback-like voltage follower (VF) circuit. Thus, $V_a = V_x$ and this voltage (i.e., $V_a = V_x$) is fed to the inverting input terminal of OTA_1 (G_{mset1}). Therefore, this OTA_1 is also operated as a VF. The voltage relationship of the EDDCC in Figure 4 can be given as follows:

$$V_x = V_{y1} - V_{y2} + V_{y3} \tag{12}$$

The addition and subtraction voltage properties of the EDDCC can be obtained.

By substituting (10) into (11), the relationship of the currents I_x and I_z can be expressed as follows:

$$I_z = \left(\frac{G_{mset3}}{G_{mset2}}\right) I_x \tag{13}$$

$$k = \frac{G_{mset3}}{G_{mset2}} \tag{14}$$

Thus, the current gain of EDDCC can be varied by adjusting the ratio of G_{mset3}/G_{mset2} ($G_{mset3}/G_{mset2} = k$).

3. Applications of the EDDCC

3.1. V-to-I Converter Using EDDCC

Voltage-to-current (V-to-I) converters, the so-called transconductors, are useful basic building blocks for realizing analog filters, oscillators, gyrators, and instrumentation amplifiers; for examples see [52–56]. In this work, the proposed EDDCC has been used to realize the V-to-I converter as shown in Figure 5. The voltage input ($V_{ind} = V_{in+} - V_{in-}$) is converted to the output current (I_{out}) by R_1 and the current gain can also be adjusted by the current gain k of the EDDCC. The circuit can work as a single-ended V-to-I converter (non-inverting or inverting input) and a differential V-to-I converter. Using (8), the output current of the circuit in Figure 5 can be expressed as follows:

$$I_{out} = k\left(\frac{1}{R_1}\right) V_{ind} \tag{15}$$

where $k = G_{mset3}/G_{mset2}$ and $V_{ind} = V_{in+} - V_{in-}$.

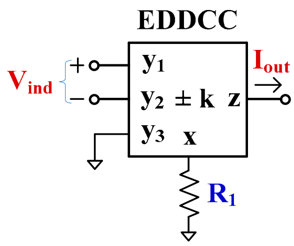


Figure 5. Applications of the EDDCC to V-to-I converter.

3.2. Current-Mode Universal Filter Using EDDCCs

To show the advantages of the current gain of the EDDCC, the EDDCC has been used to realize a current-mode universal filter as shown in Figure 6. The filter employs five EDDCCs, four resistors, and two capacitors. The output terminals possess a high impedance level, and the circuit uses grounded capacitors, which is convenient for the implementation of integrated circuits. The filtering functions can be achieved through the appropriate use of input signals and appropriate selection of output signals.

Using (8) and nodal analysis, the output currents I_{o1} and I_{o2} can be expressed as follows:

$$I_{o1} = k_5 \frac{-k_2k_3I_1 + (k_3sC_1R_T + k_1k_3)I_2}{s^2C_1C_2R_TR_3 + k_1sC_2R_3 + k_2k_3} \tag{16}$$

$$I_{o2} = k_4 \frac{k_2sC_2R_3I_1 + k_2k_3I_2}{s^2C_1C_2R_TR_3 + k_1sC_2R_3 + k_2k_3} - I_3 \tag{17}$$

where $R_T = R_1 = R_2 = R_4$.

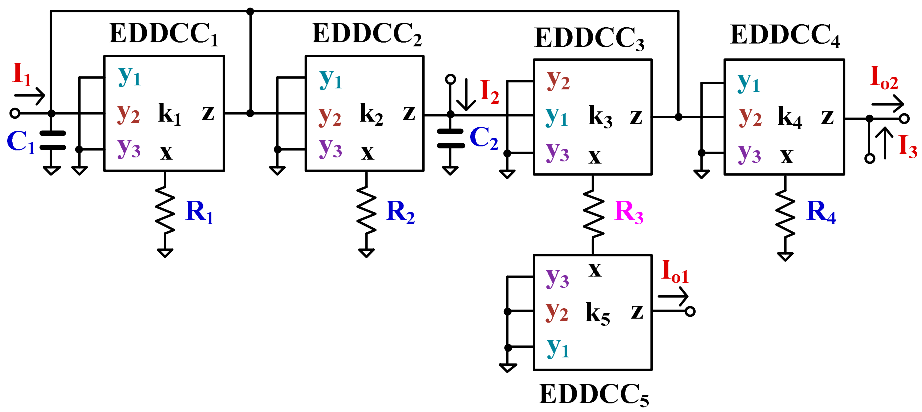


Figure 6. The proposed current-mode universal filter.

The variants of the current-mode universal filter's filtering functions are shown in Table 1. The proposed filter offers five standard filtering functions. Moreover, the current gains of LP and BP filters can be adjusted by k_4 and k_5 of EDDCC$_4$ and EDDCC$_5$.

Table 1. Obtaining variant filtering functions of the current-mode universal filter.

Filtering Function		Input	Output	Condition	Gain
LP	Inverting	I_1	I_{o1}	-	k_5
	Non-Inverting	I_2	I_{o2}	-	k_4
HP	Inverting	$I_1 = I_2 = I_3$	I_{o2}	$k_4 = 1$	1
BP	Non-inverting	$I_1 = I_2$	I_{o1}	-	k_5
	Non-inverting	I_1	I_{o2}	-	k_4
BS	Inverting	$I_1 = I_3$	I_{o2}	$k_4 = 1$	1
AP	Inverting	$I_1 = I_3$	I_{o2}	$k_4 = 2$	1

The natural frequency (ω_o) and quality factor (Q) can be expressed as follows:

$$\omega_o = \sqrt{\frac{k_2 k_3}{C_1 C_2 R_T R_3}} \quad (18)$$

$$Q = \frac{1}{k_1}\sqrt{\frac{k_2 k_3 C_1 R_T}{C_2 R_3}} \quad (19)$$

The natural frequency can be given by R_T and R_3 (i.e., R_T = R_3) and the quality factor can be controlled independently and electronically by k_1 of EDDCC$_1$. The current gains of LP outputs I_{o1} and I_{o2} can be controlled by k_5 and k_4, respectively. In the case of tuning Q of the BP, the current gain will be equal to 1 if k_1 = k_4 for output I_{o2} or k_1 = k_5 for output I_{o1}. The current gain of BP can be obtained if $k_4 > k_1$ (or $k_5 > k_1$).

3.3. Non-Ideal Analysis

Taking into account the non-idealities of the EDDCC, the relationship of the terminal voltages and currents can be rewritten as follows:

$$\begin{pmatrix} I_{y1} \\ I_{y2} \\ I_{y3} \\ V_x \\ I_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \alpha_{j1} & -\alpha_{j2} & \alpha_{j3} & 0 & 0 \\ 0 & 0 & 0 & \pm\beta_j k_j & 0 \end{pmatrix} \begin{pmatrix} V_{y1} \\ V_{y2} \\ V_{y3} \\ I_x \\ V_z \end{pmatrix} \tag{20}$$

where $\alpha_{j1} = 1 - \varepsilon_{j1v}$ and ε_{j1v} ($|\varepsilon_{k1v}| \ll 1$) denotes the voltage-tracking error from V_{y1} to V_x of the jth EDDCC, $\alpha_{j2} = 1 - \varepsilon_{j2v}$ and ε_{j2v} ($|\varepsilon_{j2v}| \ll 1$) denotes the voltage-tracking error from V_{y2} to V_x of the jth EDDCC, $\alpha_{j3} = 1 - \varepsilon_{j3v}$ and ε_{j3v} ($|\varepsilon_{j3v}| \ll 1$) denotes the voltage-tracking error from V_{y3} to V_x of the jth EDDCC, and $\beta_j = 1 - \varepsilon_i$ and ε_i ($\varepsilon_i \ll 1$) denotes the output current-tracking error of the jth EDDCC.

Using (20), the denominator of the proposed filter becomes as follows:

$$s^2 C_1 C_2 R_T R_3 + k_1 s C_2 R_3 \beta_1 + k_2 k_3 \beta_2 \beta_3 \alpha_{12} \alpha_{21} \alpha_{31} \tag{21}$$

The natural frequency and quality factor become as follows:

$$\omega_{on} = \sqrt{\frac{k_2 k_3 \beta_2 \beta_3 \alpha_{12} \alpha_{21} \alpha_{31}}{C_1 C_2 R_T R_3}} \tag{22}$$

$$Q_n = \frac{1}{\beta_1 k_1} \sqrt{\frac{k_2 k_3 C_1 R_T \beta_2 \beta_3 \alpha_{12} \alpha_{21} \alpha_{31}}{C_2 R_3}} \tag{23}$$

It follows from (22) and (23) that tracking errors change the natural frequency and the quality factor. However, it should be noted that the natural frequency can be easily compensated by adjusting k_2 and k_3 and the quality factor can be compensated by adjusting k_1.

With respect to the parasitic parameters of the EDDCC on the current-mode universal filter, the parasitic impedances R_z and C_z at the z-terminal [5] are considered. From Figure 6, it can be seen that capacitor C_1 is in parallel with parasitic capacitances C_{z1}, C_{z3} and parasitic resistances R_{z1}, R_{z3} while capacitor C_2 is in parallel with parasitic capacitance C_{z2} and parasitic resistances R_{z2}. The parasitic effects on the pole frequency of the filter can be avoided by choosing $C_1 \gg C_{z1} + C_{z3}$, $C_2 \gg C_{z2}$, $R_1 \ll R_{z1}//R_{z3}$, and $R_2 \ll R_{z2}$.

4. Simulation Results

The proposed EDDCC and its applications were simulated in the Cadence Virtuoso System Design Platform using 0.18µm CMOS technology from TSMC (Taiwan Semiconductor Manufacturing Company, Hsinchu Science Park, Taiwan). The aspect ratios of all MOS transistors of the MI-OTA in Figure 1 are listed in Table 2. The initial values of $I_{set1} = I_{set2} = 5$ µA, while the values of I_{set3} were changed to adjust the current gain k of the EDDCC.

Table 2. Parameters of the components of the MI-OTA.

Transistor	W/L (µm/µm)
M_1–M_4, M_{13}–M_{18}	10/0.5
M_{1s}, M_{2s}	5/0.5
M_5–M_{12}	20/0.5
M_R	4/5
$C_B = 0.5$ pF	
$V_{B1} = -300$ mV, $V_{B2} = 200$ mV	

For the EDDCC in Figure 3b, the supply voltage was chosen to be $V_{DD} = -V_{SS} = 0.5$ V, with the setting currents $I_{set1} = I_{set2} = I_{set3} = 5$ µA. The power consumption of the EDDCC was 90 µW. Figures 7–12 show the simulation results of the EDDCC. Figure 7 shows the ideal and simulated DC voltage characteristics V_x versus V_{y1} (V_{y2} and V_{y3} are grounded) and V_x versus V_{y2} (V_{y1} and V_{y3} are grounded) when V_{y1} and V_{y2} were swept from −0.5 V to 0.5 V. A good linearity is evident for V_X/V_{Y1} and V_X/V_{Y2} with the input voltage range ±0.3 V.

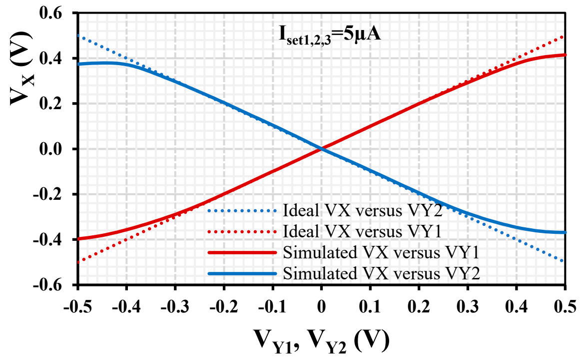
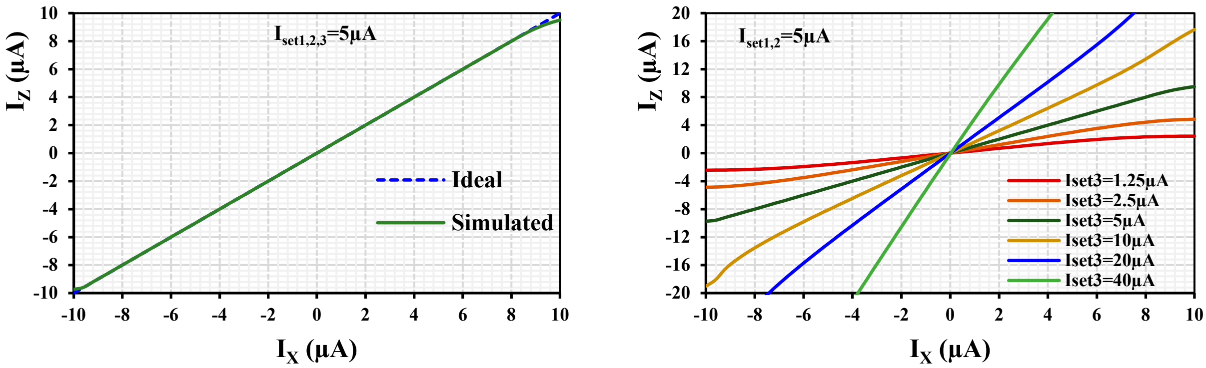
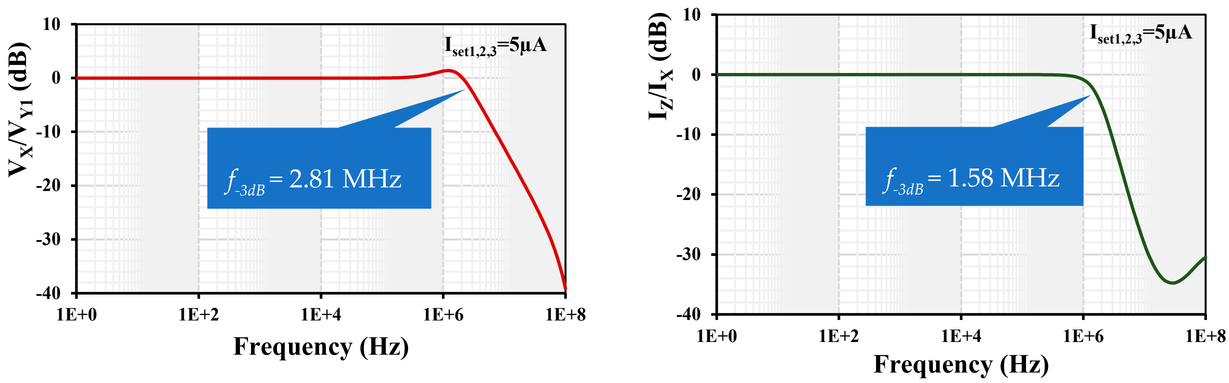


Figure 7. DC curves V_x versus V_{y1} (V_{y2} and V_{y3} are grounded) and V_x versus V_{y2} (V_{y1} and V_{y3} are grounded) showing the ideal and simulated input voltage range.



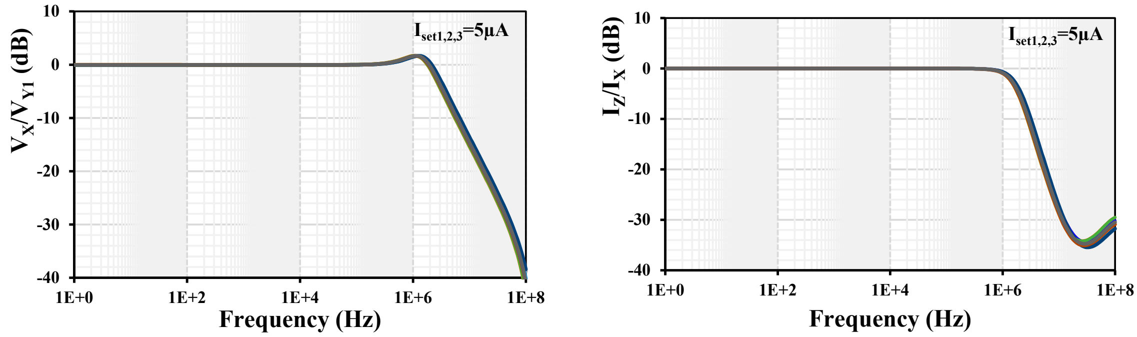
(**a**) (**b**)

Figure 8. DC curves I_z versus I_x (**a**) with k = 1 and (**b**) with different values of k.



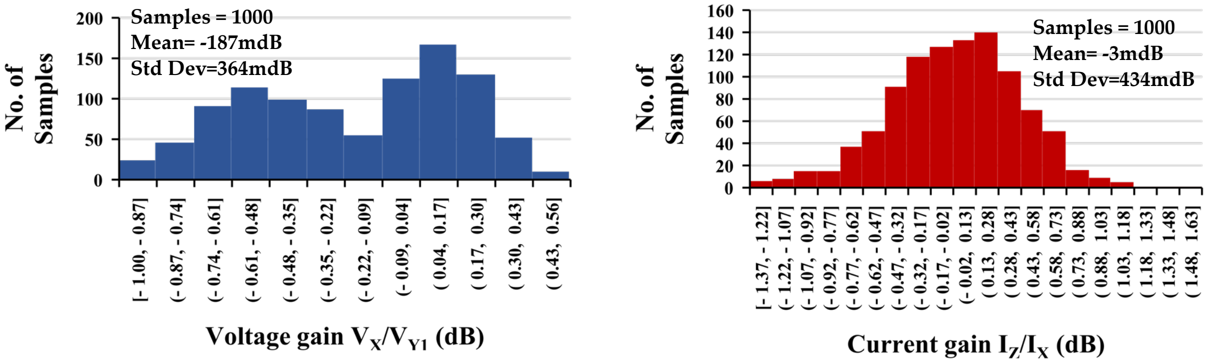
(**a**) (**b**)

Figure 9. Frequency responses of (**a**) voltage gain V_x/V_{y1} and (**b**) current gain I_z/I_x.



(**a**) (**b**)

Figure 10. Frequency responses of (**a**) voltage gain V_x/V_{y1} and (**b**) current gain I_z/I_x with PVT analysis.



(**a**) (**b**)

Figure 11. The histogram of the low-frequency (**a**) voltage gain V_x/V_{y1} and (**b**) current gain I_z/I_x with 1000 runs MC analysis.

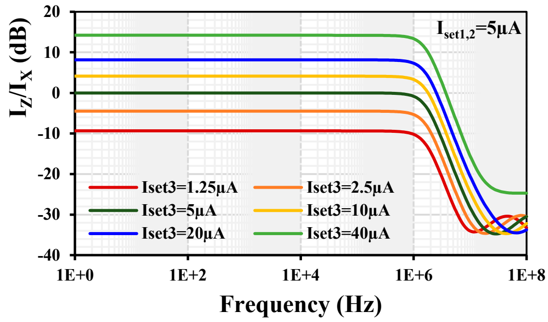


Figure 12. Frequency response of the current gain I_z/I_x with different gain k.

Figure 8a shows the ideal and simulated DC current characteristics I_z versus I_x (with k = 1) when I_X was swept from −10 µA to +10 µA. The curves overlap in the range of ±9 µA. Figure 8b shows the I_z versus I_x for different k with a constant $I_{set1,2}$= 5 µA and varied I_{set3}= (1.25, 2.5, 5, 10, 20, 40) µA. The wide turnability of I_z versus I_x is evident.

The simulated frequency responses of the voltage gain V_x/V_{y1} and the current gain I_z/I_x are shown in Figure 9. The −3 dB bandwidths were 2.81 MHz and 1.58 MHz, and the low-frequency gains were −33.6 mdB and −76 µdB for the voltage V_x/V_{y1} and current I_z/I_x gains, respectively. It is worth noting here that a compensation capacitor of 2 pF was connected between the input of G_{mset2} to obtain a flat magnitude response of the current gain. Without this compensation capacitor, the peak is around 6 dB.

Process, voltage, temperature (PVT) corners were used to confirm the robustness of the design. The process transistor corners were fast-fast, fast-slow, slow-fast, and slow-slow;

the process MIM capacitor corners were fast-fast and slow-slow; the voltage supply corners were = ±10% (V_{DD}-V_{SS}); and the temperature corners were −20 °C and 60 °C. The results for the frequency responses of the voltage gain V_x/V_{y1} and current gain I_z/I_x are shown in Figure 10. The −3 dB bandwidths were in range of (2.66 to 3) MHz and (1.49 to 1.72) MHz, and the low-frequency gains were in range of (−62.8 to 21.2) mdB and (−124.6 to 79.9) µdB for the voltage V_x/V_{y1} and current I_z/I_x gains, respectively. As is evident, the variations are within the acceptable range.

Monte Carlo (MC) analysis was used to perform the statistical analysis to estimate parametric yield and generate information about the performance characteristic of the frequency voltage gain V_x/V_{y1} and current gain I_z/I_x of the EDDCC. Figure 11 shows the histogram of a 1000 run MC analysis, showing the mean value to be −187 mdB and −3 mdB, and the standard deviation to be 364 mdB and 434 mdB for the voltage and current gains, respectively.

The simulated frequency response of the current gain I_z/I_x with a constant $I_{set1,2}$ = 5 µA and varied I_{set3}= (1.25, 2.5, 5, 10, 20, 40) µA is shown in Figure 12. The simulated current gain k was varied to (−9.3, −4.48, 0, 4.13, 8.1, 14.22) dB, respectively. This result confirms that the proposed EDDCC can provide the current gain I_z/I_x.

The simulated frequency dependence of the parasitic impedances of the z- and x-terminals is shown in Figure 13. The resistance of the z-terminal is 32.5 MΩ and the resistance of the x-terminal is 284 Ω for $I_{set1,2,3}$ = 5 µA.

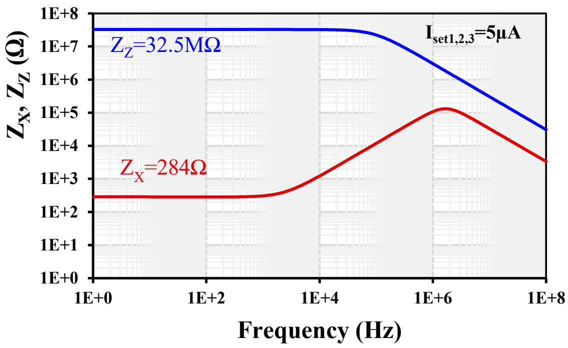
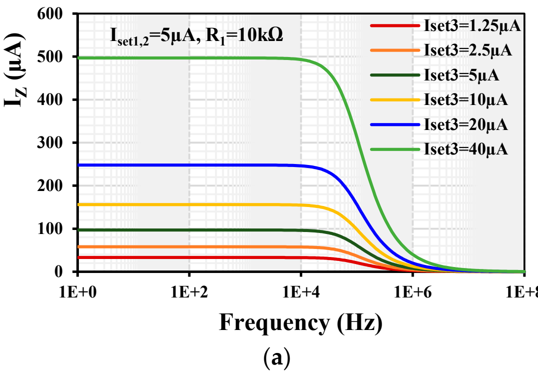


Figure 13. Frequency dependence of the parasitic impedances of x- and z-terminals.

Figure 14a shows the frequency responses of the V-to-I converter shown in Figure 5 against the current gain k for a constant R_1 = 10 kΩ, $I_{set1,2}$ = 5 µA, and various I_{set3}= (1.25, 2.5, 5, 10, 20, 40) µA, and Figure 14b for $I_{set1,2,3}$ = 5 µA and various R_1 = (2.5, 5, 10, 20, 40) kΩ. The wide tunability of the current gain is evident.



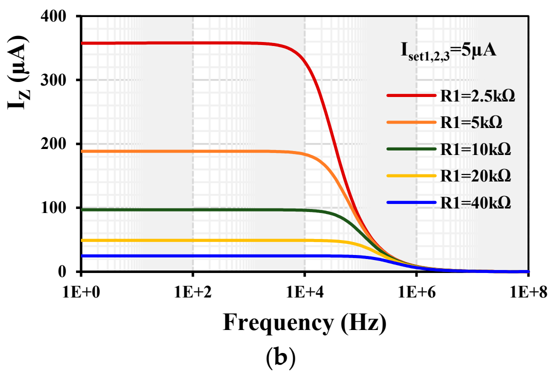


Figure 14. Frequency responses of the V-to-I converter against the current gain k for (**a**) R_1 = 10 kΩ, $I_{set1,2}$ = 5 µA, and various I_{set3}= (1.25, 2.5, 5, 10, 20, 40) µA and (**b**) for $I_{set1,2,3}$ = 5 µA and various R_1 = (2.5, 5, 10, 20, 40) kΩ.

For simulation of the current-mode universal filter shown in Figure 6, the parameters $C_1 = C_2 = 100$ pF and $R_{1–4} = 200$ kΩ were chosen. The gain $k_{1–5} = 1$ was set by choosing the setting current of all EDDCC$_{1–5}$ to be $I_{set} = 5$ µA. However, for the APF, the current of the EDDCC$_4$ was set to $I_{set3} = 13$ µA in order to obtain k = 2. The gain and phase frequency characteristics are shown in Figure 15. The cut-off frequency was 7.9 kHz.

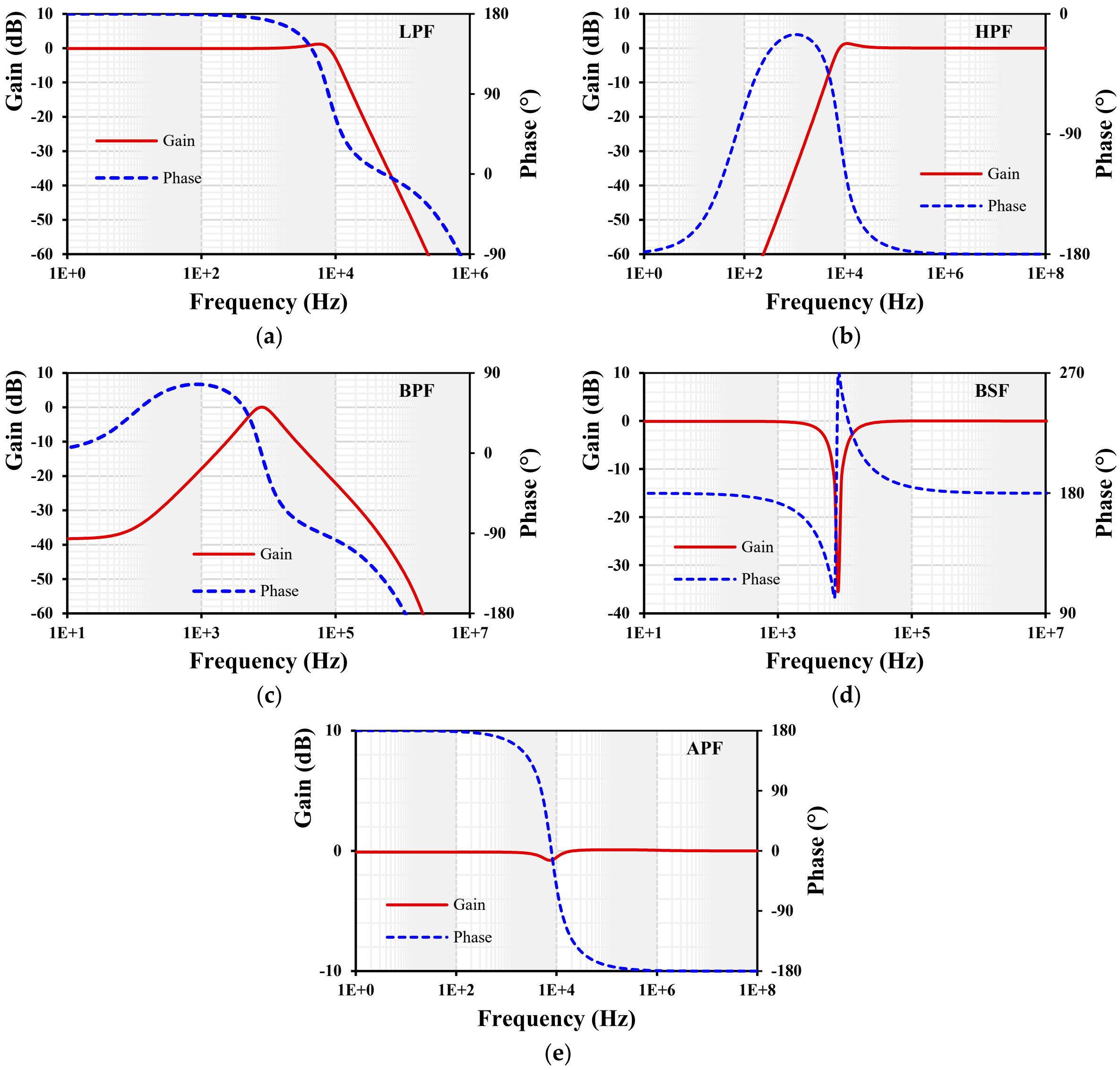


Figure 15. Gain and phase frequency responses of the current-mode filter: (**a**) LPF, (**b**) HPF, (**c**) BPF, (**d**) BSF, and (**e**) APF.

Figure 16 shows the tuning capability of the gain for the LPF and BPF. The setting current of all EDDCC$_{1-4}$ was set to be $I_{set} = 5$ µA while the k of EDDCC$_5$ was changed by its $I_{set3} = (5, 10, 20, 40)$ µA. The low-frequency gain of the LPF was around (0.1, 4, 8, 14) dB and for BPF, it was (0.02, 4.1, 8.1, 14.2) dB.

Figure 17 shows the transient response of the LPF's output (a) and the total harmonic distortion (b) when an input signal at 1 kHz and different amplitudes (0.2, 0.4, 0.6, 0.8, 1, 1.2) µA were applied to the input of the filter. The gain was set to be k = 1. The THD of the output signal was below 1.2% for an input amplitude of 1.2 µA.

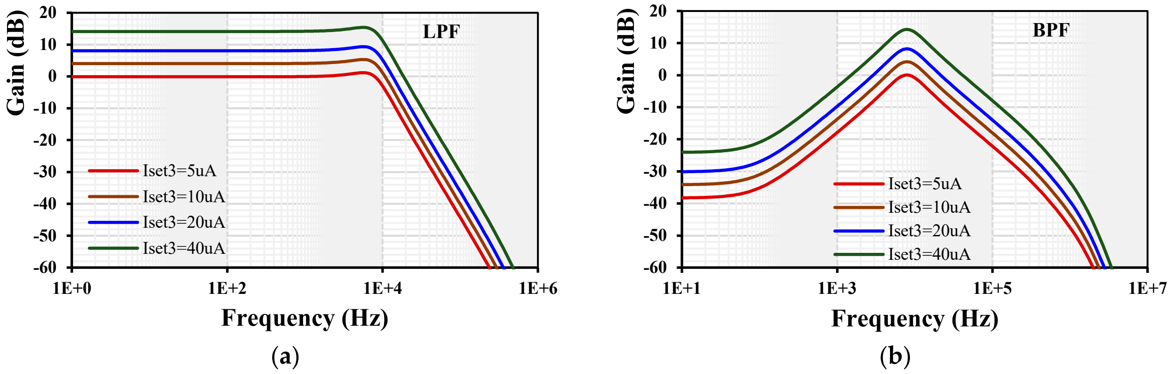


Figure 16. Gain and phase frequency responses of the current-mode filter: (**a**) LPF and (**b**) BPF.

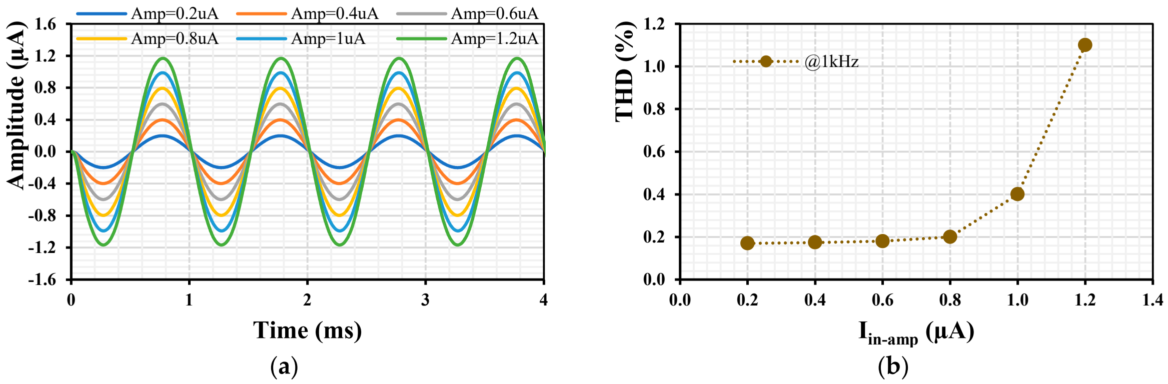


Figure 17. Transient response (**a**) and THD (**b**) of the LPF with different input signals and k = 1.

Figure 18a shows the transient response of the LPF when a sine wave I_{in} = 0.1 µA@1kHz is applied to the input of the filter with $k_{1\text{-}4}$ = 1 (I_{set} = 5 µA) while the gain k_5 of the $EDDCC_5$ is varied by its I_{set3} = (0.5, 10, 15) µA. The output signal of the LPF is inverted and amplified as expected. The THD is shown in Figure 18b, where the 0.19% THD is shown for a 0.4 µA amplitude output signal.

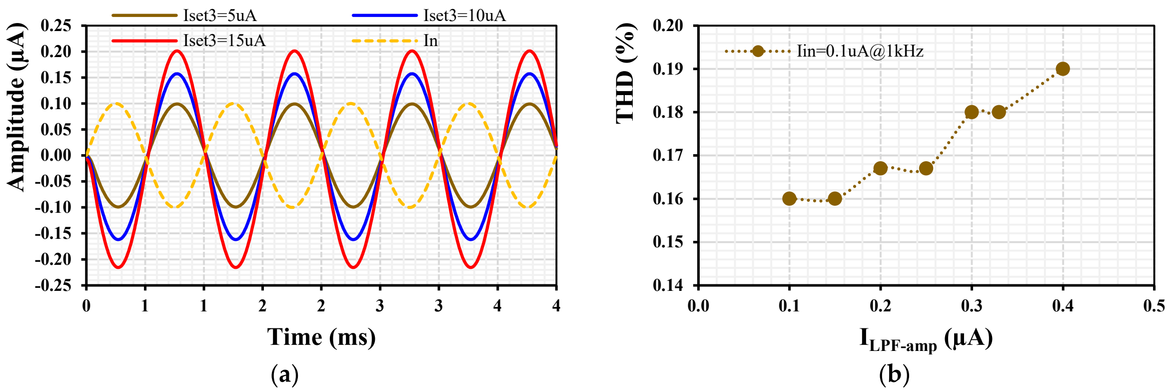


Figure 18. Transient response (**a**) and THD (**b**) of the LPF with a 0.1 µA @1 kHz input signal and various k_5.

The PVT corners analysis was also used to confirm the robustness of the filter design. The results for the gains frequency responses of the LPF, HPF, BPF, BSF, and APF with PVT are shown in Figure 19. The curves of each filter response overlap, which confirms the robustness of the filter design.

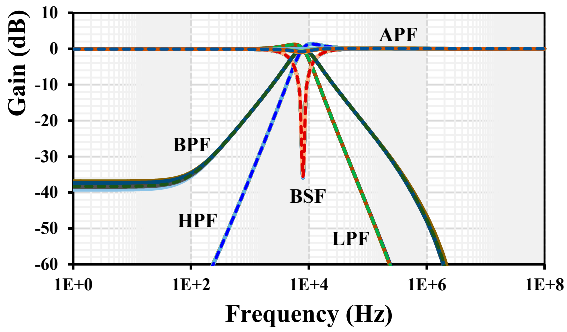


Figure 19. Gain frequency responses of the current-mode filter with PVT corners.

The proposed EDDCC was compared with previous current conveyors in [18,21,23,33,41], as shown in Table 3. Current conveyors using nonconventional techniques, i.e., the bulk-driven CCII [18], bulk-driven DDCC [21], floating-gate FDCCII [23], and current conveyors providing current gain [33,41] have been selected for comparison. Compared with the current conveyors in [18,21,23], the proposed EDDCC offers current gain between z- and x-terminals. Compared with the ECCIIs in [33,41], the proposed EDDCC has much lower power consumption and lower supply voltage. It is worth noting that the bandwidth of the proposed EDDCC is sufficient for many applications like sensors and biomedical systems.

Table 3. Properties comparison of this work with those of previously published ECCIIs.

Parameters	**Unit**	**This Work**	**[18]**	**[21]**	**[23]**	**[33]**	**[41]**
		EDDCC	**CCII**	**DDCC**	**FDCCII**	**CCII**	**CCCII**
Technique	-	BD	BD	BD	FG	GD	-
Technology	-	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.35 µm CMOS	BJT ALA400-CBIC-R
Power supply	V	±0.5	±0.4	±0.3	±0.8	±1.5	±1.5
Power consumption	mW	0.09 (90 µW)	0.064	0.0186	<3	6.6	2.2
Voltage gains: V_x/V_{y1}, V_x/V_{y2}, V_x/V_{y3}	 - - -	 0.996 0.995 0.996	 1 - -	 1 1 1	 0.94 - -	 1 - -	 0.99 - -
Current gain	-	k	1	1	1	k	k
DC voltage range	mV	−200 to 200	−380 to 380	−150 to 150	−1000 to 1000	−500 to 600	−700 to 700
Voltage offset	µV	~90	−0.4 to 0.5	<93	-	-	1.29 to −1.72
DC current range	µA	−10 to 10	−7 to 7	−8 to 8	−300 to 300	−50 to 50	−200 to 200
Current offset	nA	~−2.3	−0.9 to 0.4	<3	-	-	0.0596 to −0.0497
−3 dB bandwidth: V_x/V_{y1}, I_z/I_x	 MHz MHz	[C_L = 0.1 pF] 3.16 1.58	 14 13	 27 27	 - >1000	 107 77	 70 19
Parasitic parameters: R_x/L_x R_{y1}/C_{y1} R_z/C_z	 Ω/mH GΩ/fF MΩ/fF	 284/18.5 42/252 32.5/52	 27/860 272/117 0.89/40	 2.6 k/270 119/5 10.38/0.13	 300 - -	 46/240 ∞/2.7 73/0.35	 275/0.119 748×10^{-3}/491 814×10^{-3}/916

Note: V_x/V_{y1} = V_x/V_{y3} of CCII, GD = gate driven, BD = bulk driven, FG = floating gate.

5. Experimental Measurements

The proposed EDDCC was implemented using a commercially available LM13700 device (Texas Instruments, Dallas, TX, USA) [57]. The LM13700 IC uses a ± 15 V supply voltage and its transconductance is controlled by DC current. Since the EDDCC requires an OTA with four inputs (see Figure 4) and the LM13700 device has two inputs, the EDDCC has been implemented using four LM13700 (see Figure 20), where one provides inputs y_1 and y_2 and another provides input y_3 (the positive input of the LM13700 is y_3, while the negative input is connected to node x). Therefore, G_{mset1} transfer has been divided into G_{mset1a} and G_{mset1b} while these transfers are set to an identical value, thus, $G_{mset1a} = G_{mset1b} = G_{mset1}$. The output currents of these two OTAs are then summed in node V_a. The control of the transconductances of the LM13700 devices, in this particular implementation, is performed by the control DC voltage V_{set} (the control DC current setting transconductances is controlled by these voltages while the value of the resistor R is kept constant (32 kΩ)). The measurement has been performed using a network analyzer Agilent E5061B, generator Keysight 33500B, and oscilloscope Keysight CX3324A with a current probe CX1101A (Keysight, Santa Rosa, CA, USA). Figure 21a represents a block diagram of the used measurement setup while using the network analyzer. A simple I/V converter (shown in Figure 21b) based on a commercially available OPA860 IC (Texas Instruments) [58] has been used. Its function is as follows: the OPA860 serves as a current follower, the output current is transferred into voltage by the resistor R, and the node with the resistor R is separated from the converter output by a buffer (included in the OPA860 IC) for better impedance properties. The converter uses a supply voltage of ±5 V. A photo of the measuring workplace is depicted in Figure 22.

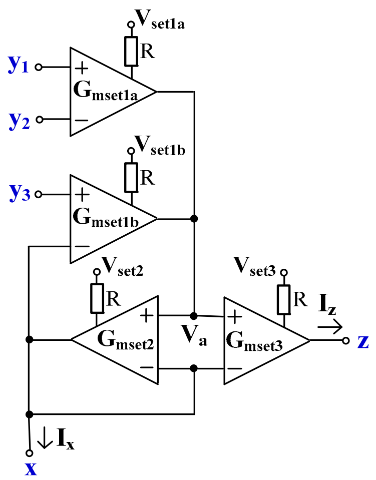


Figure 20. EDDCC using LM13700 devices.

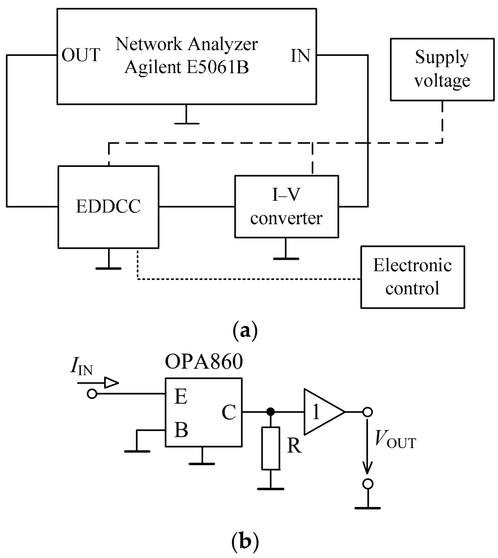


Figure 21. Block diagram of the measurement setup (**a**) and the used I/V converter (**b**).

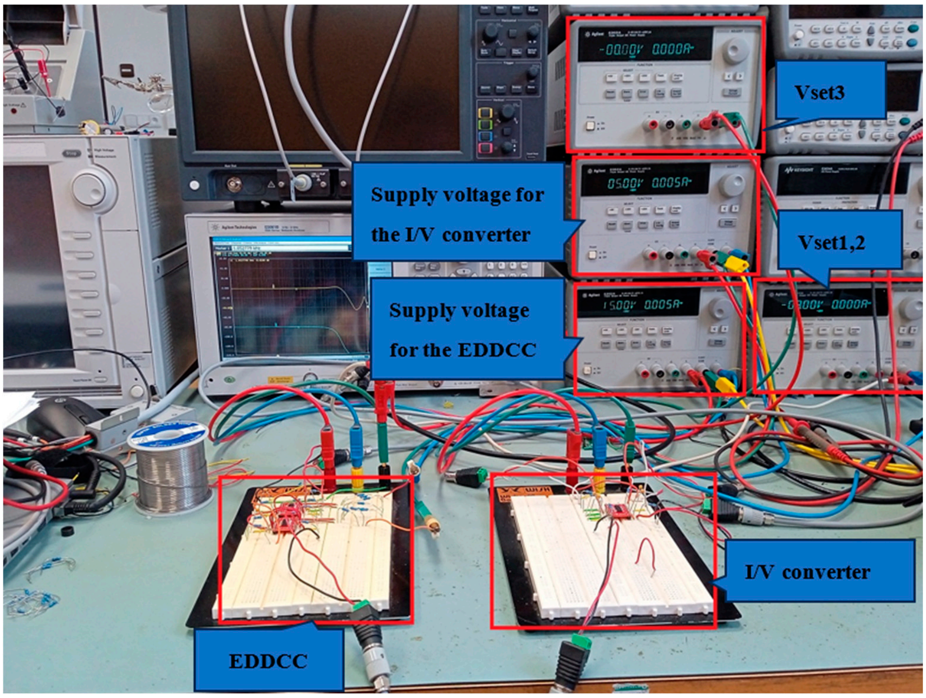


Figure 22. Experimental setup.

The default values for the measurement were selected as follows: R_x = 1 kΩ, V_{set1} = V_{set2} = −10 V, and V_{set3} = 0 V. This way, the transconductance of the EDDCC is approximately 1 mS, corresponding to the resistor (1 kΩ) used in the I/V converter for the conversion of the current from the EDDCC back to voltage, which is then fed back to the network analyzer. Note that the resulting voltage transfer corresponds to I_z/I_x transfer when taking the transfer of the I/V converter as a constant. Figure 23 shows the measured current gain I_z/I_x for the default setting. The measurement has been performed in band from 10 Hz up to 30 MHz (the analyzer bandwidth range). The −3 dB bandwidth was measured at 1.91 MHz. The gain is −0.53 dB (note that the resulting gain is given by how accurately the transfer of the EDDCC compensates the transfer of the I/V converter).

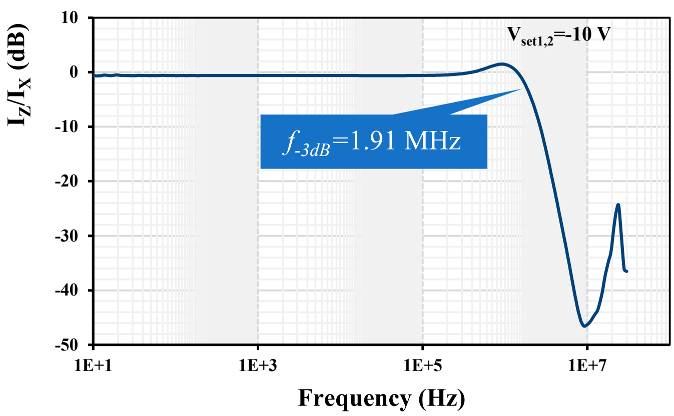


Figure 23. Measured frequency response of the current gain I_z/I_x.

The possibility to change the current gain I_z/I_x by varying V_{set3} = (−12.5, −10, −7.5, −5, −2.5, 0, 2.5, 5, 7.5, 10, 12.5) V is shown in Figure 24. The obtained current gain was (−21.11, −11.92, −7.50, −4.57, −2.37, −0.53, 0.86, 2.18, 3.11, 4,18, 5.05) dB, respectively. Figure 25 depicts the dependency of the current gain I_z/I_x on the control voltage V_{set3}. It shows a logarithmic dependency of the current gain on the control voltage based on this particular implementation.

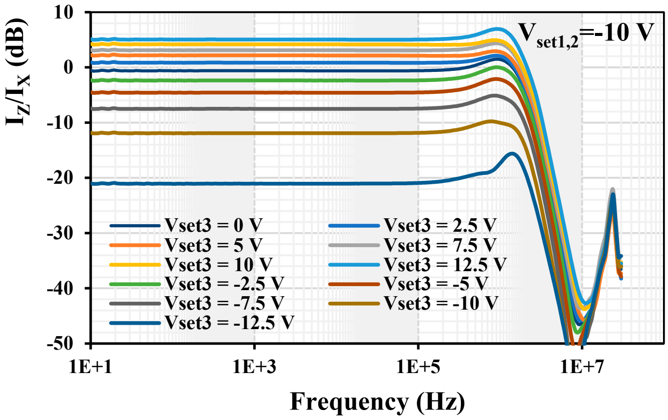


Figure 24. Measured frequency response of the current gain I_z/I_x for different values of V_{set3}.

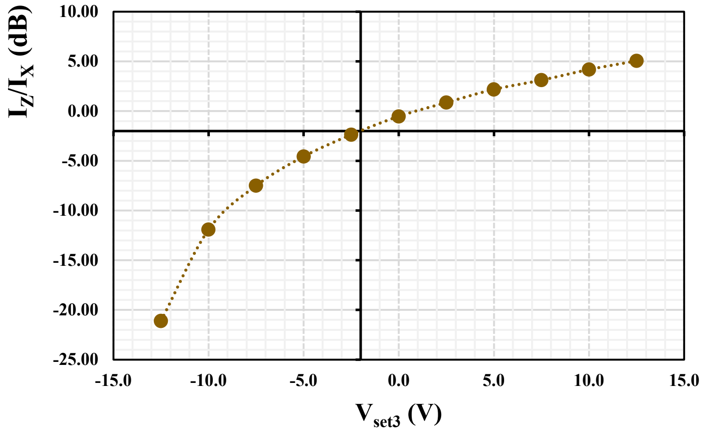


Figure 25. Dependency of current gain I_z/I_x on the control voltage V_{set3}.

The measured time domain results of voltage-to-voltage transfer (input of the EDDCC and output of the I/V converter) are presented in Figure 26. The input signal measured at the input of the EDDCC had an amplitude of 57 mV and frequency of 1 kHz. The output signal for V_{set3} = (−12.5, −10, −7.5, −5, −2.5, 0, 2.5, 5, 7.5, 10, 12.5) V is (6, 15, 26, 35, 44, 55, 66, 76, 85, 97, 107) mV, which provides the gain (−19.55, −11.60, −6.85, −4.24, −2.25, −0.31, 1.27, 2.50, 3.47, 4.62, 5.47) dB. There is a 180° of the output in comparison to the input given by the I/V converter (its transfer is inverting). These values correspond well with the values of the current gain I_z/I_x obtained by the analyzer.

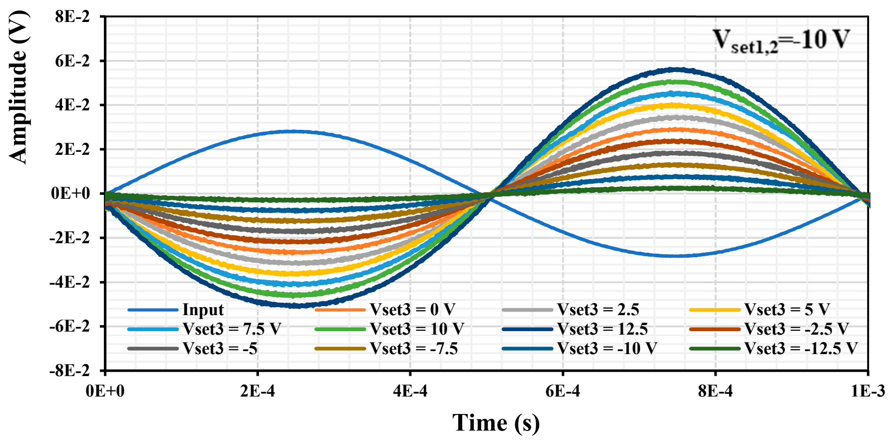


Figure 26. Measured time domain responses for different values of V_{set3}.

6. Conclusions

In this paper, a new low-voltage low-power electronically tunable current conveyor has been proposed. Unlike previous current conveyors, the current gain of the proposed current conveyor can be controlled electronically. The proposed current conveyor can work as an electronically tunable DDCC (EDDCC) and an electronically tunable CCII (ECCII). To show the advantages of the current gain of the proposed current conveyors, the V-to-I converter and current-mode universal filter were presented, and the simulation results confirm the functionality of the proposed circuits. The proposed EDDCC uses ±0.5 V power supply, consumes 90 µW of power, and has a ±200 mV DC voltage range, ±10 µA DC current range, and 90 µV voltage offset. The proposed circuit can also offer a 2.81 MHz bandwidth of the voltage gain V_x/V_y, a 1.58 MHz bandwidth of the current gain I_z/I_x, and a current gain of −9.3 to 14.22 dB when the bias current is varied from 1.25 µA to 40 µA. In addition, the experimental measurements of the EDDCC further support the concept and its functionality.

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